Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N.1R**
2. **1D**
3. **1CP**
4. **N.1S**
5. **1Q**
6. **N.1Q**
7. **GND**
8. **N.2Q**
9. **2Q**
10. **N.2S**
11. **2CP**
12. **2D**
13. **N.2R**
14. **VCC**

**.054”**

**.056”**

**12**

**11**

**10**

**9**

**1 14 13**

**2**

**3**

**4**

**5**

**6 7 8**

**HCR74E**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Vcc**

**Mask Ref: HCT74E**

**APPROVED BY: DK DIE SIZE .054” X .056” DATE: 8/26/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HCT74**

**DG 10.1.2**

#### Rev B, 7/19/02